REMARKS

Reconsideration of the application is requested.

Applicant acknowledges the Examiner's acceptance of the drawings filed on November 13,2000 and the continued confirmation of receipt of applicant's certified copy of the priority document for the German Patent Application 199 54 346.1, filed November 11, 1999 supporting the claim for priority under 35 U.S.C. § 119.

The applicant also appreciatively acknowledges the Examiner's withdrawal, in item 1.2 on page 1 of the above-identified Office Action, of the objections and rejections previously of record in response to Applicant's Amendment of January 6, 2004 and respectfully requests similar reconsideration of the instant Amendment.

Claims 1-27 are in the application. Claims 1-27 were rejected in the above-identified Office Action. Claims 1 and 10 have been amended.

In "Title" item 2 on page 1 of the above-identified Office Action, the Examiner objected to the title of the invention because "the current title is imprecise" and is not "indicative of the invention" to which the claims are

directed, namely "the use of comparator units in memory addressing." The Examiner's suggested corrections have been made.

In "Claim Rejections - 35 USC § 112 SECOND PARAGRAPH" item 3.0 on page 1 of the above-identified Office Action, claims 1-27 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, in item 3.1 the Examiner states:

> it is unclear to the Examiner how the memory device is operatively connected, e.g., how the memory cells, the comparison units and address applied to the memory device are linked to perform intended functionality.

Moreover, the Examiner expressed additional clarity concerns regarding, "how the comparison units are placed in the testing state."

Although the Examiner's assumption that the "address is applied to the comparator units" is correct, Claim 1 has been amended in an effort to clarify how the comparison units, memory cells, and the address are connected to perform the intended functionality.

Support for these changes may be found on pages 11 and 12 of the specification of the instant application. Additional support may be found in FIG. 1 and FIG. 5, which are

described on pages 1-4 and 11-20 of the specification of the instant application.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In "Claim Rejections - 35 USC § 102" item 4.1 on page 2 of the above-identified Office Action, claims 1-27 have been rejected as being fully anticipated by U.S. Patent No. 6,202,180 to *Nose* (hereinafter **NOSE**) under 35 U.S.C. § 102(e).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 13 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be

helpful. Claim 1 calls for, *inter alia*, a memory device including:

> a multiplicity of memory cells for storing data;
>
> comparison units connected to said memory cells and **each having an address input** for receiving an address applied to the memory device, said comparison units being configured **to simultaneously check** whether the address applied to the memory device is associated with **at least one memory cell which cannot be properly written to or read out** or **to simultaneously check** whether the address applied to the memory device is located in **a memory cell area containing memory cells which cannot be properly written to or read out**, and
>
> in a testing phase of the memory device, said comparison units being placed into **a testing state different from a state during a normal operation** of the memory device.

Thus, the comparison units of the instant application are individually assigned to specific memory cells or memory cell areas. The comparison units operate in parallel so that the addresses applied to the memory device are, in each case, **compared simultaneously by all comparison units** with the reference addresses associated with each active comparison unit, that is to say **simultaneously with all reference addresses.** not in claim 1

As explained on page 20, each comparison unit may be individually activated or deactivated. In this way the comparison units described in the instant application are more like a bit level check or block level check than those more general tests shown in **NOSE**.

For example, in "**a testing state**" the comparison units may be individually activated and deactivated to verify the integrity of at least one memory cell or memory cell area. The comparison units may be associated with at least one reference address for the testing state and the normal state. Once the testing is completed, memory cells that fail the testing can be registered for future redirection. Upon registering the failed memory cells, the comparison units return to their "**state during a normal operation**" or normal state.

The **NOSE** reference discloses a semiconductor memory for a display capable of relieving a defective memory cell by exchanging addresses. More specifically, the converting circuit outputs the address stored in a second memory circuit when an address supplied from an external address input coincides with the address stored in a first memory circuit. As mission critical semiconductor memory, display memory should be checked regularly to ensure a proper display. Accordingly, a self-test circuit 14 in **NOSE** operates at power-on time and the like to test the memory operations of all memory addresses (col. 5, lines 12-15). The self-test circuit provides the address, the writing data, and the expected value to check the memory operations of the main

memory 16. Any address found to be faulty is stored in memory circuit 13. After the self-test, the memory checks the address of a requested memory and if it matches then the spare memory 17 is activated and the data is stored or retrieved from the spare memory 17, depending on the nature of the original request.

Clearly, **NOSE** does not show comparison units "to simultaneously check" whether a received address is associated with at least one memory cell or memory cell areas that cannot be properly written as recited in claim 1 of the instant application.

Moreover, in one embodiment described in claims 10 and 11, the received address is compared with a "registered" reference address that is at least partially permanently in the memory device. Claim 11 notes that the registration is accomplished through a "plurality of fuses" that define the registration of the reference addresses. **NOSE** explicitly teaches against the use of fuses (Col. 1, lines 17-23) as "leading to an increase in manufacturing cost" and requiring additional programming and processing overhead. As such, **NOSE** does not teach or suggest that "reference addresses associated with at least one of the testing state and the normal state of said comparison units can be **registered** at

least partially permanently in the memory device" as recited in claim 10 of the instant application. Nor does **NOSE** show "a plurality of fuses defining the registration of the addresses" as recited in claim 11 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-27 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

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